REMARKS

Claims 1-24 are pending. Claims 1, 6, 14, 15, 16, and 22 are being amended. Claims 5 and 11 are being canceled without prejudice or disclaimer of the subject matter recited therein. Claims 25 and 26 are being added. No new matter is being added.

Claim 12 stands rejected under 35 U.S.C. Section 112. This rejection is now moot with the amendment to claim 6.

Appreciation is expressed for the allowance of claim 15. Claim 15 is being amended for clarity. Furthermore, claims 1, 14, 16, and 22 are being amended for clarity. These amendments are being made for clarity are not being made for patentability purposes.

Claims 1-4, 6-10, 11-13, 16-21, and 23-24 stand rejected under 35 U.S.C. 102(e) as being anticipated by Okuno, U.S. Patent No. 6,105,114 (Okuno). Claims 5, 11, 14, and 22 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Okuno in view of Lee et al., U.S. Patent No. 5,920,504 (Lee). These rejections are traversed for at least the reasons set forth below.

Pending claim 1 has been amended to incorporate limitations of dependent claim 5. Claim 5 has been canceled without prejudice or disclaimer of the subject matter recited therein.

Claim 5 was rejected in Section 6 of the Office Action. Section 6 states that Okuno fails to teach a plurality of nonvolatile memory cells. Section 6 states that Lee teaches a plurality of nonvolatile memory cells. Section 6 further states that "it would have been obvious to one having ordinary skill in the art at the time of the invention was made to use a nonvolatile memory, wherein the nonvolatile memory is able to conserve data even when there is no power supply, as thought by Lee into [the] system of Okuno in order to preserve data from erasure in case of [a] power shortage."

Applicants respectfully submit that amended claim 1 is allowable over Okuno and Lee in that one of ordinary skill in the art would not have been motivated to use the nonvolatile memory array of Lee in the memory circuit of Okuno for at least the reasons given below.

Okuno discloses a transposition memory circuit 1 used for performing two-dimensional array transposition of blocks of NxN pixel data to implement a two dimensional discrete cosine transform (DCT). Okuno, column 1, lines 8-25, column 4, lines 5-9, and column 7, lines 31-47. Circuit 1 of Okuno includes a memory cell array 2 in which data can be written to and read from simultaneously and independent of each other. Okuno, column 10, lines 1-6. Accordingly, when the reading of data (e.g. one pixel) from a cell for a first block of data (of NxN pixel data) is complete, data from a next block of data can be written to the cell. See Okuno, column 9, line 51 to column 10, line 16 where it describes how data from a first block (data that was previously written) is read from the memory cells of array 2 while data from a second block is written to the memory cells of array 2. See also Okuno, column 10, lines 17 to column 10, line 34 where it describes how data from the second block is read from the memory cells of array 2 while data from a third block is written to the memory cells. For accomplishing these operations, memory cell array 2 is responsive to a clock signal for writing data to a memory cell at a rising edge of a clock signal and reading data from a memory cell at a falling edge of a clock signal. Okuno, column 7, lines 48-66.

The ability to perform the operations above enables circuit 1 to perform the transportations of a two dimension array of data with one memory cell array and without using two memory cell arrays. Okuno column 4, lines 32-40; column 5, lines 5-12; column 5, lines 40-42; column 6, lines 6-9 and lines 50-52; and column 11, lines 27-35. The ability to perform these operations without two memory arrays is enabled by the use of a memory array having

memory cells that can be written to and read from simultaneously. See Okuno, Column 5, lines 25-27 and lines 44-46; column 6, lines 10-14 and lines 51-54; column 8, lines 37-40; and column 10, lines 1-6. The ability of circuit 1 of Okuno to perform the desired operations without two memory arrays results in reducing circuit scale and power consumption. Okuno, column 4, lines 38-40; column 5, lines 12-14; column 6, lines 21-23 and lines 56-58; and column 11, lines 31-36. Also, such a memory array enables the circuit to have the same processing speed as conventional circuitry. See Okuno, column 5, lines 47-49; column 6, lines 14-15 and lines 24-26, and column 6, lines 54-56.

One of ordinary skill in the art would not be motivated to include the nonvolatile memory taught in Lee in the circuit of Okuno because Lee does not teach that its memory array can be written to and read from simultaneously and independently of each other.

Lee discloses a nonvolatile memory such as a flash EEPROM. Lee, column 1, lines 5-13. Lee does not disclose that its nonvolatile memory is a cell array in which data can be written to and read from simultaneously and independently of each other. For example, the nonvolatile memory of Lee requires that a program voltage (e.g. 18 volts) or an erasure voltage (e.g. 20 volts) be applied during program or erase operations wherein a read voltage of e.g. 4.5 volts is applied during read operations. Lee, column 4, lines 1-5 and column 7, line 10. Accordingly, one of skill in the art could not implement circuit 1 of Okuno with the flash EEPROM of Lee in that the flash EEPROM of Lee can not be operated this way. Thus, memory circuit 1 of Okuno modified to include the flash EEPROM of Lee could not perform the transposition operations as set forth in Okuno. See MPEP Section 2143.01, Subsection THE PROPOSED MODIFICATION CANNOT RENDER THE PRIOR ART UNSATISFACTORY FOR ITS

INTENDED PURPOSE and the subsection entitled THE PROPOSED MODIFICATION CANNOT CHANGE THE PRINCIPLE OF OPERATION OF A REFERENCE.

Furthermore, as set forth above, Okuno teaches a desirability for processing speed. Lee does not teach that its flash EEPROM is capable of delivering the same speed (especially in a erase or program operations) as array 2 of Okuno in performing the transposition operations set forth in Okuno. Accordingly, one of skill in the art would not be motivated to modify circuit 1 of Okuno with the flash EEPROM of Lee in that it would decrease operating speed.

Furthermore, Okuno explicitly teaches away from the use of a memory like that set forth in Lee. Okuno explicitly teaches that its objective is to reduce power consumption, and more specifically, reduce power by lowering "the supply voltage or the like." Okuno, column 3, lines 60-64. However, Lee teaches that program voltages of 18 volts and erasure voltages of 20 volts are needed with the memory of Lee for programming and erasing memory cells of the nonvolatile memory array of Lee. Lee, column 4, lines 1-4. Accordingly, one of skill in the art would be not be motivated to use the flash EEPROM of Lee in the circuit of Okuno in that the memory array of Lee requires relatively high voltages (e.g. 18 V and 20 V) for writing as with respect to its read voltages (e.g. 4.5 V) and that Okuno specifically teaches against using such high voltages.

As set forth above, Okuno also teaches the desirability to reduce circuit scale. However, implementing the nonvolatile memory array of Lee in circuit 1 of Okuno would require that circuit 1 of Okuno include an Erasure/Program Control Circuit 30, Erase Voltage Generator 32, and Program Voltage Generator 33. Accordingly, one of skill in the art would not be motivated to modify the circuit of Okuno to include the flash EEPROM of Lee in that it would require that

circuit 1 of Okuno have extra circuitry (including extra circuitry operating at higher voltages), which is explicitly taught away from in Okuno.

Section 6 of the Office Action states that one of skill in the art would have been motivated to use the nonvolatile memory as taught by Lee in the system of Okuno in order to preserve data from erasure in case of a power shortage. Applicants respectfully submit that this reason would not motivate one of skill in the art to combine the flash EEPROM of Lee in the system of Okuno.

First, Okuno teaches a transposition circuit for implementing a transforming coding technique using a two-dimensional discrete cosine transform for coding image data such as MPEG data. Okuno, column 1, lines 8-25. Okuno implements a transposition memory circuit 1 for performing these operations. Okuno, column 7, lines 31-47. The circuit of Okuno is used for decoding multiple blocks of image data with a read and write operation being performed to each cell of array 2 for each block of data being processed. Okuno, column 7, line 31- column 8, line 36.

Nowhere in Okuno does it require circuit 1 of Okuno to be able to store data when the power is off, nor is there any suggestion of it being desirable to save the data in memory array 2. In fact, memory array 2 is not utilized to store data for any substantial period of time. Okuno appears to teach that data is only "stored" in memory array 2 during a cycling of the addresses as provided by counter 20 to perform the transposition operations. See Okuno, column 8, lines 9-13 and in general column 9, line 31 – column 10, line 34. Since circuit 1 is part of a coding system for image data, there is no need to store data in array 2 when circuit 1 does not have power in that circuit 1 would not be used to encode data when there is no power. Because there is no need to store data in array 2 of Okuno (other than for a short period of time during a transposition

operation), there is no reason for one of skill in the art to modify Okuno to include a nonvolatile memory of Lee for the purpose of saving data during a power outage.

In addition, because the system of Okuno requires multiple reads and writes of the same cells for processing data, one of skill in the art would not be motivated to include a flash EEPROM as taught in Lee due to the limited number of lifetime read and write cycles of such memories.

Accordingly, because 1) Okuno teaches that its systems uses an array in which data can be written to and read from simultaneously and independently of each other, and the nonvolatile memory of Lee does meet this requirement; 2) because Okuno explicitly cites the desirability of speed, low power (due to low voltage), circuit minimization, and multiple reads and writes, and the use of the nonvolatile memory of Lee would actually provide a significantly reduced performance in each of these areas; and 3) because the ability to save the data in memory array 2 of Okuno during a power outage is not a requirement or even desirable, one of skill in the art would not be motivated to modify the circuit of Okuno with the nonvolatile memory of Lee. Accordingly, amended claim 1 is allowable over Okuno and Lee.

Claim 6 has been amended to include the limitations of pending claim 11. Pending claim 11 has been canceled without prejudice or disclaimer of the subject matter recited therein. Amended claim 6 recites "the array of storage elements comprises a plurality of nonvolatile memory cells," and therefore is allowable over Okuno and Lee for at least for reasons similar to those given above with respect to amended claim 1.

Pending claim 14 recites "an array of nonvolatile memory cells." Accordingly, amended claim 14 is allowable over Okuno and Lee for at least reasons similar to those given above with respect to amended claim 1.

Pending claim 16 has been amended to include "wherein the array of addressable storage elements comprises a plurality of nonvolatile memory cells." Accordingly, amended claim 16 is allowable over Okuno and Lee for at least the reasons similar to those given above with respect to amended claim 1.

Pending claim 22 and newly added claim 25 each recite "an array of nonvolatile memory cells." Accordingly, pending claim 22 and newly added claim 25 are allowable over Okuno and Lee for at least reasons similar to those given above with respect to amended claim 1.

Each dependent claim depends from an independent claim and is allowable for at least this reason.

The application is believed to be in condition for allowance and notice of such is respectfully requested. If there is any remaining issues, the Examiner is respectfully requested to telephone the undersigned.

If Applicant has overlooked any additional fees, or if any overpayment has been made, the Commissioner is hereby authorized to credit or debit Deposit Account 503079.

Respectfully submitted,

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